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A2

to permit the anti-fuse portion to be broken with a reasonably low voltage while suppressing the damage done to the judging circuit and other portions as much as possible.

The paragraph starting on page 9, line 20, has been amended as follows:

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It is possible to form the second gate electrode on the bottom surface of the third concave portion, on both side surfaces or one side surface of the third concave portion, and on the semiconductor substrate.

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The paragraph starting on page 14, line 17, has been amended as follows:

FIG. 22A is a plan view showing the case where a gate electrode for a plurality of anti-fuses is formed in a single concave portion;

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The paragraph starting on page 14, line 22, has been amended as follows:

FIG. 23A is a plan view showing the case where a concave portion is filled with a gate electrode for an anti-fuse and a contact is formed on an element isolating region;

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The paragraph starting on page 19, line 16, has been amended as follows:

According to the first embodiment of the present invention described above, the gate insulating film 18 for the anti-fuse is formed on a bottom surface of the third concave portion 14. It should be noted that damage is done to the bottom surface of the third concave portion 14 by the RIE process employed for forming the concave portions 12, 13 and 14. Therefore, it is possible to lower the breakdown voltage of the gate insulating film 18b formed in the concave portion 14, compared with the gate insulating film 18a of the transistor formed on the surface of the substrate 11. It follows that it is possible to break only the gate insulating film 18b for the anti-fuse without applying an extremely high voltage. This makes it possible to suppress the damage done to the gate insulating film 18a of the transistor included in, for example, a judging circuit portion. It follows that it is possible to maintain a high reliability of the transistor and to improve the yield.

The paragraph starting on page 21, line 2, has been amended as follows:

*A7* For example, where the lower end portion of the resist film 17 is positioned inside the upper edge portion of the third concave portion 14, it is possible to permit the silicon oxide film 15 to remain partly within the third concave portion 14, as shown in FIG. 7. It should be noted that, in the step of forming the gate electrode, damage is done to the gate insulating film in the edge portion of the gate electrode in the step of, for example, the RIE process, making it impossible to adjust completely the nonuniformity in the breakdown voltage of the gate electrode. However, in the structure shown in FIG. 7, the remaining silicon oxide film 15 resides in the edge portion of the gate electrode 24. It follows that the breakdown at the edge portion of the gate electrode 24 can be suppressed by the insulating film formed of the silicon oxide film 15, making it possible to adjust the nonuniformity in the breakdown voltage of the gate insulating film 18b.

The paragraph starting on page 22, line 16, has been amended as follows:

*A8* According to the second embodiment, the corner portions 14a and 14b of the concave portion 14 are used as the anti-fuse. Therefore, the electric field concentration occurs on particularly the corner portions 14a and 14b so as to make it possible to break effectively the gate insulating film 18b.

The paragraph starting on page 24, line 8, has been amended as follows:

*A9* It should be noted that the polysilicon film 19 and the silicon nitride film 21 are formed in many cases by, for example, an LPCVD (Low Pressure Chemical Vapor Deposition) method that is carried out under high temperatures, e.g., several hundred °C. Therefore, stress derived from the difference in the thermal expansion coefficient is generated under room temperature under which the semiconductor device is actually used. It follows that the breakdown voltage of the anti-fuse portion can be further lowered, compared with the semiconductor device shown in, for example, FIGS. 8 and 9. It should also be noted that, since the gate electrode 24 extends onto the silicon substrate 11, the gate electrodes 22 and 24 for the transistor and the anti-fuse could be formed in the same height in the lithography step for forming the gate electrodes 22 and 24. This

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facilitates the lithography step and further improves the yield. Incidentally, the structure shown in FIG. 12 produces the effect that a position alignment between the contact plug 28 and the tungsten film 20 is easy, compared with the structure shown in FIG. 11.

*A10*  
The paragraph starting on page 25, line 12, has been amended as follows:

In each of the first and second embodiments of the present invention described above, the silicon oxide film 15 within the concave portion 14 is removed completely in the stepping process shown in FIG. 3. However, it is not absolutely necessary in the present invention to remove completely the silicon oxide film 15 within the concave portion 14. For example, it is also possible to leave the silicon oxide film 15 unremoved in a part of the concave portion 14, as shown in FIG. 14. In this case, even if damage is done to the bottom surface of the concave portion 14 in the RIE step for forming the concave portion 14, it is possible to suppress the nonuniformity in the breakdown voltage of the gate insulating film by forming the silicon oxide film 15 on the bottom surface of the concave portion 14 after formation of the concave portion 14.

*A11*  
The paragraph starting on page 26, line 10, has been amended as follows:

Also, as shown in FIG. 15, it is possible to form the contact plug 28 for the electrical connection to the gate electrode (not shown) of another element above the element isolating region 16. Where a contact hole is formed on an element region, damage is done to the gate insulating film right under the contact hole in the RIE step for forming the contact hole, giving rise to a possibility of generating a nonuniformity in the breakdown voltage. In the case of the structure shown in FIG. 15, however, it is possible to suppress the nonuniformity in the breakdown voltage derived from the damage generated in the step of forming the contact hole because the contact hole is formed above the element isolating region.

*A12*  
The paragraph starting on page 27, line 26, has been amended as follows:

As shown in FIG. 18, the conductivity type, e.g., P-type, of a well 32a formed in a surface region of the silicon substrate 11 is made equal to that of a polysilicon film 19a. As a

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*A12*

result, it is possible to lower the resistance of the anti-fuse portion after breakdown of the gate insulating film 18b so as to improve the accuracy of judgment of breakdown/non-breakdown.

*A13*  
The paragraph starting on page 28, line 22, has been amended as follows:

Also, as shown in FIG. 20, the conductivity, e.g., N-type, of the well 32b formed in a surface region of the silicon substrate 11 is made equal to that of the polysilicon film 19b, and the impurity concentration in the polysilicon film 19b is made higher by at least one place than that in the well 32b. Incidentally, in this apparatus, a positive electric field is imparted to the gate electrode 24 in breaking down the gate insulating film 18b in the anti-fuse portion, and a negative electric field is imparted to the gate electrode 24 when the apparatus is actually used for performing the judgment. Where the polarities of the electric field in the breakdown step and the judging step are made opposite to each other, the depletion layer formed in the well 32b on the lower side of the gate is thickened in the judging step because the impurity concentration in the well 32b is lower than that in the polysilicon film 19b. As a result, only an effectively low electric field is applied to the gate insulating film in the anti-fuse portion that was not broken down. It follows that it is possible to increase the reliability of the judging operation that is repeatedly performed in actually using the apparatus.

*A14*  
The paragraph starting on page 31, line 2, has been amended as follows:

Also, the damaged layer in the uppermost surface of the silicon substrate 11 can be removed by etching thin the surface of the silicon substrate 11 by an isotropic etching such as a CDE (Chemical Dry Etching) method in removing the silicon oxide film 15 in the stepping process shown in FIG. 3. It is also possible to weaken the effect of the electric field concentration by rounding the corner portions 14a and 14b of the concave portion 14. The breakdown voltage rendered lower than a predetermined value can be restored to some extent by these methods, too.

*A15*  
The paragraph starting on page 31, line 13, has been amended as follows:

By contrast, where it is desired to further lower the breakdown voltage, it is possible to further introduce damages to the bottom surface of the concave portion 14 by using a RIE method having a high power in place of the wet etching method in removing the silicon oxide film 15 in the stepping process.

*A16*  
The paragraph starting on page 31, line 19, has been amended as follows:

Further, after removal of the silicon oxide film 15 in the stepping process, an impurity ion is introduced by using the ion implantation technology before the resist film 17 is peeled off. As a result, it is possible to control the thickness of the gate oxide film 18 formed in the subsequent process. It follows that it is possible to control the breakdown voltage of the gate insulating film 18b. For example, after the lithography process for the stepping, a nitrogen ion implantation is performed. Thereby it is possible to form the thin thickness of the gate oxide film 18 formed in the subsequent process, it is possible to gain the breakdown voltage of the predetermined value by the film 18 being used as anti-fuse. In this case, the stepped portion of the anti-fuse portion is not always a necessity, however it is possible to lower the breakdown voltage by the stepped portion.

*A17*  
The paragraph starting on page 33, line 26, has been amended as follows:

In general, a capacitor element is formed in many cases within the semiconductor device for stabilizing the power source. In this embodiment, used is a capacitor formed of a gate insulating film 48, as shown in FIG. 26. For further stabilizing the power source, it is necessary to form a capacitor having a larger capacitance within the semiconductor device. However, in recent years, the area occupied by the capacitor for stabilizing the power source has been rendered large relative to the area of the entire chip so as to increase the manufacturing cost of the semiconductor device. Such being the situation, it is required to diminish the area occupied by the capacitor for stabilizing the power source.